UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,649	12/29/2000	Ashok Singhal	M-8495 US	9244

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EXAMINER
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 September 2008</u>.
2a)☐ This action is **FINAL**.　　　　2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-3 and 10-13</u> is/are pending in the application.
　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) <u>1-3,10-13</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on <u>29 December 2000</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.
　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
　　a)☐ All　b)☐ Some * c)☐ None of:
　　　1.☐ Certified copies of the priority documents have been received.
　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.
　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

In view of the Appeal Brief filed on 9/25/2008, PROSECUTION IS

HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of

the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a

reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31

followed by an appeal brief under 37 CFR 41.37. The previously paid notice of

appeal fee and appeal brief fee can be applied to the new appeal. If, however,

the appeal fees set forth in 37 CFR 41.20 have been increased since they were

previously paid, then appellant must pay the difference between the increased

fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening

prosecution by signing below.

Response to Arguments

Applicant's arguments filed 9/25/2008 have been fully considered but they

are not persuasive.

Applicant argues that Steely Jr. et al. does not disclose a memory copy write command that mirrors data in a line of memory at a local node to a corresponding line of memory at a remote node after the line of memory at the local node has been written.

The Examiner asserts that the reflective memory that is written to in Steely is a part of the local memory. In other words, even though writing to the reflective memory maps the data to addresses at other nodes, Steely is still writing to memory in a local node. For example, see Fig. 9A, in which it is shown that reflective memory 77b is included in local memory 77a. Writing to addresses in 77b reflects the data to addresses in 87b.

Regarding claim 11, Applicant argues that the prior art does not teach the steps of calculating parity and writing the parity from a local node to a remote node combined under a single command.

The Examiner notes that the "single operation" claimed in claim 11 could comprise more than a single command. The Authoritative Dictionary of IEEE Standards Terms defines "operation" as: An action defined by a procedure.

Applicant argues with respect to claim 1 that Steely does not disclose or suggest that an entire page at a node is mirrored to another node when less than the entire page is written.

The Examiner notes that Steely teaches a reflected memory write between nodes in col. 6, lines 46-47 and col. 7, lines 13-15. In a reflected

memory write, written data is reflected to the other nodes. Steely discloses that

connection granularity between nodes is at the page level (col. 4, lines 54-57),

which means that the smallest unit of data transmitted between nodes is 8k bytes

in the example in col. 4, lines 54-57. Therefore, data smaller than 8k bytes that

is written to memory will still be transmitted in a page of 8k bytes by using pad

bits or any other method commonly known in the art. This makes sense because

memories operate on units of data- in this particular case 8k bytes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described
> as set forth in section 102 of this title, if the differences between the subject matter sought to
> be patented and the prior art are such that the subject matter as a whole would have been
> obvious at the time the invention was made to a person having ordinary skill in the art to which
> said subject matter pertains. Patentability shall not be negatived by the manner in which the
> invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1,

148 USPQ 459 (1966), that are applied for establishing a background for

determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at
     issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
     obviousness or nonobviousness.

1.   Claims 1-3 10, 12, and 13 rejected under 35 U.S.C. 103(a) as being

unpatentable over Steely, Jr. et al (US Pat. 6,049,889; hereafter referred to as

Steely) in view of Grivna (US Pat. 5,850,556) in view of Ebrahim (US Pat.

5,887,134) in view of Dann (US Pat. 4,991,079). Lawlor et al (US Pat.

6,038,677) is relied upon in claim 13 as a teaching reference to show that which

was well known in the art.

As per claim 1:

Steely teaches a communication link protocol for communicating between

a local node and a remote node of an interconnect system via a communication

link, the communication link protocol comprising:

- a direct memory access (DMA) command for performing an inter-node

  transfer of a block of data directly from the local node to the remote node

  via one of the communication links (col. 4, lines 15-20 explains the

  reflective memory design of Steely as mentioned in col. 6, line 46. Dann

  in an analogous art further teaches the reflective memory design in col. 4,

  lines 56-63. Data written to the network address space is copied to the

  other units 11 and 13);

- an administrative write command for writing data from the local node to

  registers in the remote node via the communication link for administrative

  purposes (col. 5, lines 36-45);

- a memory copy write command for copying an entire line of memory from

  a local node to a corresponding line of memory at the remote node via one

  of the communication links after a new data is written into the line of

  memory at the local node even when the new data is smaller than the line

  of memory at the local node (col. 6, lines 46-47; col. 7, lines 13-15; Steely

  teaches in col. 4, lines 54-57 that the memory address space is divided

into N pages of data, where each page is 8 kilobytes of data. Therefore, it

is clear that data must be transmitted in pages of 8k bytes because Steely

states that "connection granularity between nodes in the network is at the

page level". When data smaller than 8k bytes is written into the memory

address space, the entire 8k bytes of data must be transmitted because

that is the page size as indicated by Steely).

Not explicitly disclosed by Steely is an inter-node DMA transfer of a block of

data directly from a local node to a remote node. However, Ebrahim in an

analogous art teaches memory mapped computer network nodes that employ

DMA operations to transfer messages between nodes (col. 7, lines 21-30).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time the invention was made to use DMA to transfer data in the system of

Steely. This modification would have been obvious to one of ordinary skill in the

art, at the time the invention was made, because one of ordinary skill in the art

would have recognized that the page aligned DMA operation detailed by Ibrahim

(col. 2, lines 46-48) could have been used in the page aligned memory structure

of Steely (col. 4, lines 54-58) in order to free the CPU to perform other operations

as stated by Ibrahim in col. 2, lines 52-53.

Also not explicitly disclosed by Steely is a built in self test (BIST) command

for testing the functionality of the communication link. However, Grivna teaches

a communication system which uses a BIST testing logic for testing the

functionality of the communication link (col. 6, lines 52-56). Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention

was made to combine a BIST testing architecture as described by Grivna with the system of Steely to issue a BIST command for testing the functionality of the communication link. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that BIST would have provided the advantage of allowing diagnostics of the communication link, as described by Grivna in column 6, lines 52-56.

As per claim 2:

Steely further teaches the communication link protocol of Claim 1 wherein each command is conveyed between the local node and the remote node in the form of a respective command packet (col. 9, lines 8-9).

As per claim 3:

Steely further teaches the communication link protocol of Claim 2 wherein each respective command packet carries information for at least one command flag (col. 9, lines 18-23; the DV bits are a command flag that dictate the occurrence of an idle cycle).

As per claim 10:

Steely further teaches the communication link protocol of Claim 1, wherein said performing an inter-node DMA transfer of a block of data directly from the local node to the remote node comprises copying the block of data from a local memory of the local node to a remote memory of the remote node (col. 8, lines 41-43).

As per claim 12:

Steely further teaches the memory copy write command of claim 12 as detailed above in claim 1 in col. 4, lines 54-57 and col. 7, lines 13-15 in which existing data is necessarily read, new data merged in a page, and then written and transferred in a reflected memory write to the remote location.

As per claim 13, the Examiner asserts that it was well known to identically replicate data of a local node at a remote node. For example, Lawlor et al (US Pat. 6,038,677) teaches that a cluster configuration is which each component is mirrored to ensure redundancy in the even that one node fails is well known in the art (col. 1, lines 14-27).

2.   Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Steely in view of Grivna in view of Ibrahim as applied to claim 1 above, and further in view of Gunsaulus et al (US Pat. 5,914,970; hereinafter referred to as Gunsualus).

As per claim 11:

Steely, Grivna, and Ibrahim teach the communication link protocol of claim 1 above. Not explicitly disclosed is said writing a block of data from a local node to a remote node comprises computing parity over multiple blocks of data from a local memory of the local node and writing the parity to a remote memory of the remote node. However, Gunsaulus in an analogous art teaches computing parity for a number of memory devices and writing the parity in one dedicated memory device (col. 1, lines 46-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to compute parity over multiple blocks of data and write the parity to a remote memory of the remote node. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using one memory device for parity storage reduces the number of memory devices needed for storing parity, as disclosed by Gunsaulus in col. 1, lines 52-55.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVE NGUYEN whose telephone number is (571)272-7214. The examiner can normally be reached on M-F, 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-

9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/   Steve Nguyen
Supervisory Patent Examiner, Art Unit 2114   Examiner
                                                            Art Unit 2117

Conferee:

Cynthia Britt
/CB/